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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/003,180

10/30/2001

Heon-Deok Park

9898-197

4103

7590

10/20/2004

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EXAMINER

KERVEROS, JAMES C

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/003,180

Applicant(s)

PARK ET AL.

Examiner

JAMES C KERVEROS

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 May 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-20 are pending and are hereby presented for examination, in response to AMENDMENT filed 5/28/2004.
2. The objection to the abstract of the disclosure, for not complying with the proper language and format, is hereby withdrawn, in view of the correction made by the amendment.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Okayasu (US 6157200).

Regarding independent Claims 1, 8, 12, 16, and dependent claims 17-20, Okayasu discloses a semiconductor device test system and method, Figures 1, 4 and 5, comprising:

A plurality of comparator and driver units, such as an analog comparator group 104 and a driver group 103 in the pin electronics 102, Figure 1, each comparator 104

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and driver unit 103 comprising a driver 103A for driving an input signal from the pattern generator 201 to be applied to a (terminal P) of the DUT, and a comparator 104A configured to compare data output from one or more output pins P of the semiconductor device DUT with a predetermined output signal pattern H and L logic, also shown in Figure 5, which illustrates the pin unit 110 in the FIG. 4. The comparison results by the analog comparator group 104 are sent via response signal transmission lines 302 back to the tester main frame 200, wherein they are logically compared by a logical comparator 203 with expectation patterns (EPD) from the pattern generator 201 to detect a mismatch between them and consequently a failing part.

A plurality of control units, (relay matrix 105) for switching the device groups (103 and 104) connected to respective terminals of the DUT, where each control unit (105) configured to electrically connect a corresponding comparator 104A and driver unit 103A to a pin (terminal P) of the semiconductor device DUT in response to a control signal from a local pin controller 111, wherein pins (P) of the semiconductor device DUT are divided into pin groups corresponding to device groups (103 and 104), where each pin group having K number of pins, and where ($K > 1$) is an integer greater than 1.

A pattern memory (201) for storing the input signal patterns and the output signal patterns expectation patterns (EPD), Figures 1 and 4.

Regarding Claims 2 and 3, Okayasu discloses that each control unit is a multiplexer (relay matrix 105) for switching the device groups that are connected to respective terminals of the DUT having ($K > 1$) of inputs (P), configured to receive control signal via a data bus. The control signal is stored in the register group 111D,

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which is input into the relay control circuit 111F to control the pin electronics 102A and the relay matrix 105 to put them in the state corresponding to the test mode.

Regarding Claims 4-7, 9-11, 13-15, Okayasu discloses output and input pins corresponding to signal RX and TX. A memory, such as pattern memory (201) located in an external device (200) tester main frame, for storing input patterns and output expectation patterns (EPD), Figures 1 and 4.

Response to Arguments

4. Applicant's arguments, see pages 7 and 8 under remarks, filed 5/28/2004, with respect to the rejection(s) of claim(s) 1-20 under 35 U.S.C. 102(b) as being anticipated by Conner (US 5794175) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of claims 1-20 rejection under 35 U.S.C. 102(e) as being anticipated by Okayasu (US 6157200).

5. In response to applicant's argument, with respect to claimed limitation recited in claims 1 and 8, that Conner does not disclose electrically connecting a corresponding driver and comparator unit to a pin of the DUT, the Examiner agrees with the Applicant's argument. However, under the new grounds of rejection, Okayasu discloses control unit (relay matrix 105) for electrically connecting a corresponding comparator 104A and driver unit 103A to a pin (terminal P) of the semiconductor device DUT using switching action by a control signal from a local pin controller (111).

The Examiner agrees with the Applicant's argument that Conner does not disclose a memory for output patterns nor input patterns, in claim 12, which recites a broad limitation of "a pattern memory comprising an input pattern memory and an output pattern memory". However, under the new grounds of rejection, Okayasu discloses a pattern memory (201) for storing the input signal patterns and the output signal patterns expectation patterns (EPD), Figures 1 and 4.

The Examiner finds applicant's argument persuasive, with respect to Claim 16, that Conner does not disclose "connecting a pin of the test system to a pin of the semiconductor device (DUT). However, under the new grounds of rejection, Okayasu discloses connecting a pin (terminal P) of the semiconductor device (DUT) through I/O module (113) of the pin unit 110 with RX or TX corresponding to a pin of the test system (200) tester main frame.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

JP 11190761 A, PUB-DATE: July 13, 1999. Waveform inspection device for analyzing defect in semiconductor integrated circuit including the claimed limitations of control units Relays (22, 24); arbitrary test signal driver (35); Response signal comparator (36) and DUT (39). Test signal from several drivers (35) are given to DUT (39) whose response signals are then given to comparator (36) through a relay (24). The testing signals are also output to comparator through relay (22).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.


Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 5 October 2004
Office Action: Non-Final Rejection

By: 

JAMES C KERVEROS
Examiner
Art Unit 2133


GUY J. LAMARRE
PRIMARY EXAMINER